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CPT Cesium-Cell Atomic Clock Operation With a 12-mW Frequency Synthesizer ASIC

Yazhou Zhao, Steve Tanner, Arnaud Casagrande, Christoph Affolderbach, Luc Schneller, Gaetano Mileti, and Pierre-André Farine

***Abstract*— In this paper, we present the design, fabrication, and electrical characterization of a low-power microwave source for interrogation of cesium atomic hyperfine transition frequency using the coherent population trapping (CPT) technique. The 4.6-GHz frequency generation and signal buffering is performed by a single-chip frequency synthesizer ASIC with a frequency tuning resolution of 1×10^{-13} and a programmable RF output power from -10 to 0 dBm. The circuit was used to modulate the current of a vertical-cavity surface-emitting laser through a dedicated impedance matching network and low thermal conductivity transmission line. Strong modulation sidebands with >60% of carrier amplitude were obtained with an ASIC power consumption of 12 mW. The system was used as optical source for atomic interrogation in an experimental cesium CPT clock. The measured clock stability of 5×10^{-11} at $\tau = 1$ s, going down to 4.5×10^{-12} at $\tau = 200$ s, is limited by the signal-to-noise ratio of the detected CPT signal.**

***Index Terms*— Atomic clocks, cesium, frequency synthesizers, microwave circuits, phase locked loops (PLLs).**

I. Introduction

MODERN wireless communication and navigation systems depend on stable frequency references for synchronization and positioning. Atomic clocks are mostly used for this purpose, and are being miniaturized to be deployed in a large scale or used in portable applications, such as global navigation satellite system (GNSS) receivers and future mobile communication devices. The miniature atomic clocks offer reduced dimensions ($\sim$10 cm^3), low power consumptions (approximately hundreds of mW) [1], [2] and are good candidates for low-cost mass production.

A low phase noise, high resolution microwave frequency synthesizer is a required component for performing low-noise interrogation in atomic clocks. For battery-powered systems, low power operation is also needed. Different topologies of frequency synthesis for atomic interrogation have been proposed. One technique, depicted in [3], employs frequency multiplication with step recovery diodes (SRDs); the approach in [4] is based on a frequency chain using sampling mixers to avoid narrow-band filtering; in [5] and [6], nonlinear transmission line circuits are used instead of SRD for frequency multiplication. The power consumption of these techniques, as well as their size, is not suited for miniature atomic clocks. On the contrary, frequency synthesizers based on fractional-N phase-locked loop (PLL) controlling an LC voltage-controlled oscillator (VCO) have been used in miniature atomic clocks thanks to their high frequency tuning resolution, low phase noise, low power consumption, and ability for full integration. For example, in [1] and [7] a 4.6-GHz synthesizer for a miniature coherent population trapping (CPT) clock is built using discrete components, reaching a power consumption of 40 mW and giving a clock short-term stability of $5 \times 10^{-11}\ \tau^{-1/2}$, limited by the RF synthesizer phase noise. In [8], a fully integrated 3.4-GHz frequency synthesizer for rubidium CPT clocks is shown, featuring 25 mW of power consumption and a frequency tuning resolution of 10^{-12}. The clock short-term stability was measured to be $4 \times 10^{-10}\ \tau^{-1/2}$. Finally, in [9] is presented an original scheme based on an injection-locked VCO featuring a 6$\times$ clock multiplication from a 569-MHz VCXO to reach the 3.4 GHz of rubidium, and consuming only 6 mW, but realized with discrete components.

This paper presents the design, fabrication, and characterization of a low-power microwave system for CPT atomic interrogation, based on a fully integrated 4.6-GHz fractional-N PLL frequency synthesizer [10] and on an RF subsystem performing optimal power transmission from the synthesizer to a thermally isolated vertical-cavity surface-emitting laser (VCSEL). Stability measurements of an experimental atomic clock operated with the present frequency synthesizer are given. A short-term stability of $5 \times 10^{-11}\ \tau^{-1/2}$ is measured, while the frequency synthesizer ASIC consumes only 12 mW and reaches a frequency tuning resolution of 1×10^{-13}, allowing in turn the same accuracy for the absolute frequency tuning of the complete clock.

This paper is organized as follows. In Section II, the specifications and architecture of the circuit are presented. Section III details the circuit design. Section IV provides experimental results of the chip, while Sections V and VI give results of the circuit used in atomic clock applications.

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Y. Zhao, S. Tanner, and P.-A. Farine are with the Electronics and Signal Processing Laboratory, Ecole Polytechnique Fédérale de Lausanne, Neuchâtel CH-2000, Switzerland (e-mail: pierre-andre.farine@epfl.ch).

A. Casagrande is with Asulab SA, Marin-Epagnier 2074, Switzerland (e-mail: acasagrande@asulab.ch).

C. Affolderbach, L. Schneller, and G. Mileti are with the Laboratoire Temps-Fréquence, Université de Neuchâtel, Neuchâtel CH-2000, Switzerland (e-mail: gaetano.mileti@unine.ch).

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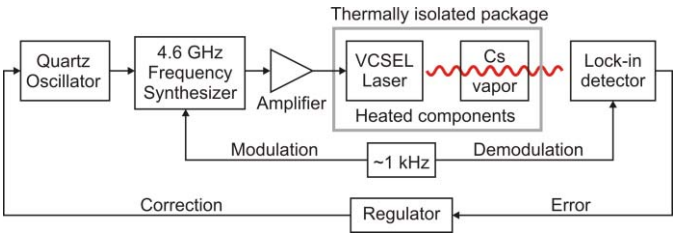

Fig. 1. Atomic interrogation loop of a CPT-based clock.

II. System Specification

The general diagram of a cesium CPT atomic interrogation loop is shown in Fig. 1. In order to achieve the desired excitation and interrogation of the atoms, the current of a thermally stabilized VCSEL laser is modulated at 4.6 GHz, creating two optical sidebands separated by the 9.2-GHz ground-state hyperfine transition frequency of cesium. The CPT signal is detected using a photodetector and a lock-in amplifier operated in the kHz range, the modulation being applied to the synthesizer's frequency. This scheme sets the general requirements for the RF frequency synthesizer. First, it has to generate a 4.6-GHz frequency signal with sufficient RF power for VCSEL laser diode current modulation. The selected VCSEL requiring -5 to -8 dBm of RF input power, and considering the transmission losses, a maximal differential ASIC RF output power of 0 dBm was selected, and was set adjustable over 10 dB to accommodate for variations in laser modulation efficiency and component impedance.

Second, its output frequency must be tunable with a high resolution so that the relative frequency error remains significantly smaller than the targeted clock stability. In the present case, a tuning step of 10^{-3} Hz was selected so as to ensure a frequency stability below 1×10^{-12}. Third, the RF signal must be modulated in frequency with a rate and a depth of typically 1 kHz in order to be used in a lock-in amplifier configuration. Fourth, the synthesizer must feature a low phase noise level; due to the intermodulation effect [11], its phase noise at higher order harmonics of the modulation frequency f_m results in a limit to the clock frequency stability given by

$$\sigma_y(\tau) = \sqrt{\sum_{n=1}^{\infty} C_{2n} \cdot S_\varphi(2nf_m)} \cdot \tau^{-1/2} \tag{1}$$

where $\sigma_y(\tau)$ is the Allan deviation [12] as function of the averaging time τ, n is the harmonic number, S_φ is the phase noise measured at even harmonics of the modulation frequency, and C_{2n} is the sensitivity coefficient given by

$$C_{2n} = \frac{2n}{(2n-1)(2n+1)} \frac{f_m}{\nu_{\mathrm{Cs}}} \tag{2}$$

where $\nu_{\mathrm{Cs}} = 4.6$ GHz is the synthesizer output frequency (half of the Cs hyperfine splitting). Using $f_m = 1$ kHz, considering a constant phase noise at harmonic frequencies, and looking for a high-performance clock stability of $\sigma(\tau) = 2 \times 10^{-11}\ \tau^{-1/2}$, the calculated phase noise at the 4.6-GHz output should be below -80 dBc/Hz, for frequency offsets ranging from the modulation frequency f_m and over the whole PLL bandwidth.

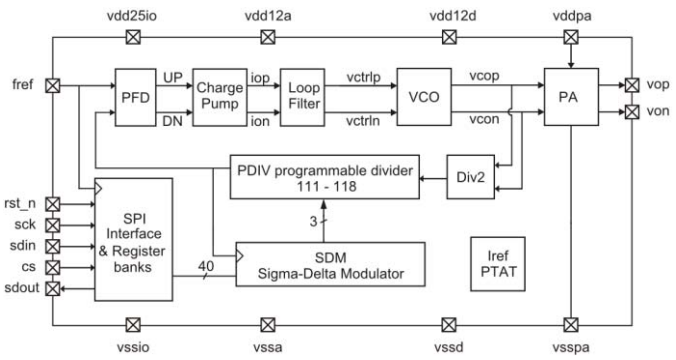

Fig. 2. Frequency synthesizer ASIC general architecture [10].

In order to achieve the performance constrained by the limited power consumption and size, an all-integrated approach was chosen. Its general architecture is shown in Fig. 2, taken from [10]. It consists of a direct generation of the 4.6 GHz using a VCO whose output frequency is controlled by a PLL, which includes a phase and frequency detector (PFD), a charge-pump (CP), a loop filter, and a 4.6-GHz VCO. Its output is first divided by 2 (Div2 block), and then feeds PDIV, a programmable divider (111–118) controlled by a sigma-delta modulator (SDM) [13], [14]. The VCO output drives a power amplifier (PA) with integrated low dropout regulator (LDO) for programmable output power. A proportional to absolute temperature (PTAT) reference is present on-chip. All chip functions are fully controlled through a register bank and a serial peripheral interface.

The oscillator is a 4.6-GHz LC-VCO known for its low power consumption and low phase noise. In order to satisfy the high frequency resolution, the PLL includes a fractional frequency divider in the feedback loop. This is done by employing an SDM controlling the division ratio of a programmable divider. The quantization error introduced by the integer divisions is pushed to high frequencies thanks to the noise shaping properties of the SDM. It is then filtered out by the loop filter and does not degrade the phase noise.

III. Circuit Design

The circuit design was fully presented in [10]. This section concentrates on the PA, not previously described.

The PA allows driving a differential output load of 100 Ω with a maximal output power of 0 dBm. The top-level schematic diagram of the PA is shown in Fig. 3(a). It is a differential Class C amplifier, implemented with a differential integrated inductor at the output node. The bias current sources and main amplifier transistors are combined ($M2$ and $M4$, W/L of 768/0.12 μm). $C3$ and $C4$ (0.21 pF) are the ac coupling input capacitors, while $R2$–$R5$ (40 kΩ), $M5$ and $C5$ form the biasing circuit. $M1$ and $M3$ are used as cascode transistors and have the same size as $M2$–$M4$. $C1$ is used to stabilize the LDO output presented later on. $R1$–$C2$ is used to filter the VDD voltage applied to the cascode transistors. An internal impedance of 500 Ω at each inductance node is selected, and depends on the available quality factor of the inductor, amounting to 20. The bias current is 10% of each

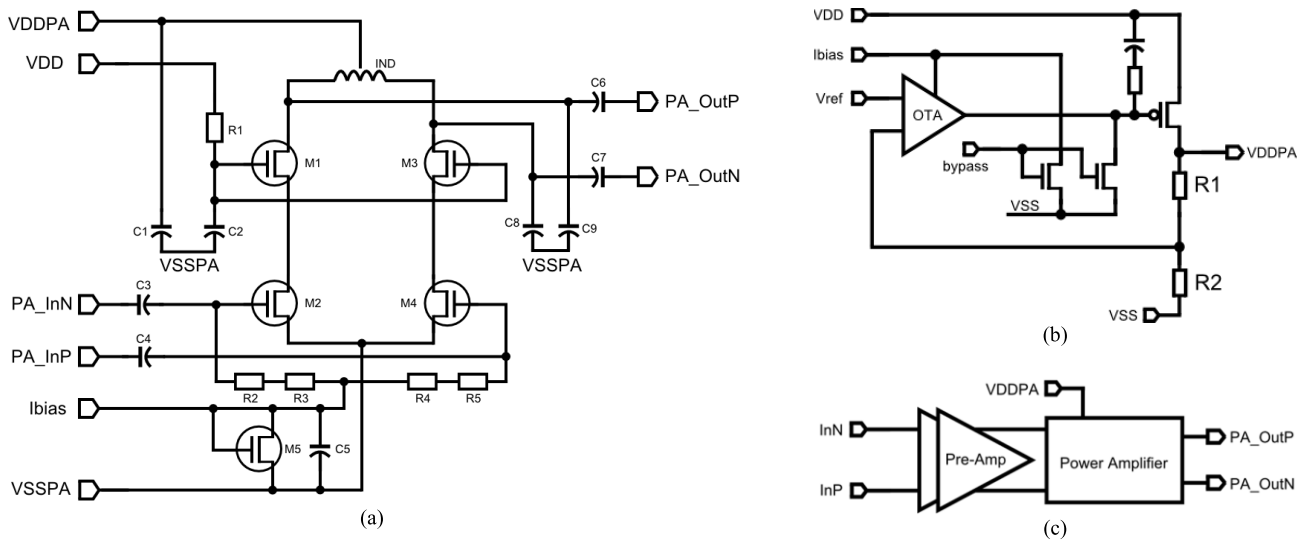

Fig. 3. (a) Schematic diagram of the PA. (b) LDO regulator for PA. (c) PA with preamplifiers.

branch active current, and can be programmed between 20 and 160 μA. The theoretical PA efficiency is 33%.

In order to adapt the PA output to the external impedance load of 50 Ω (100-Ω differential), a capacitive coupling network made of $C6$–$C7$ (0.2 pF) and $C8$–$C9$ (0.3 pF), and of the parasitic of the RF pad with ESD protection diode (0.4 pF), is used. The programmable RF output power between 10 and 0 dBm is achieved by varying the PA supply voltage by means of an integrated LDO regulator whose schematic diagram is shown in Fig. 3(b). $R2$ can be digitally programmed with a 6-bit R–$2R$ ladder from $1 \times R1$ to $64 \times R1$.

The regulator stability is achieved with a one pole one zero RC structure, and the operational transconductance amplifier is rail-to-rail input type. The main output filtering capacitor is capacitor $C1$ of the PA.

Before applied to the PA, each VCO asymmetrical signal is preamplified by means of two dc-biased ac-coupled CMOS inverter stages, shown in Fig. 3(c), the second one having a doubled transconductance. The overall PA preamplifier current consumption is 1.8 mA. Post-layout simulations give a maximal efficiency of PA preamplifier and amplifier of 23%.

IV. Circuit Realization and Experimental Results

The frequency synthesizer was designed and implemented into a 130-nm RF CMOS process. A microphotography is shown in Fig. 4. The PLL+PA active area measures 0.7 mm^2. Its left side contains the VCO inductor, while the PA inductor is located on the right, with two RF output pads, and a ground pad in the middle. The whole RF layout was drawn strictly symmetrical. The rest of the chip area contains other test structures not described here.

A. VCO Characterization

The VCO was characterized alone using differential test input pads for VCO control voltages. Fig. 5 shows the output frequency as a function of the differential input control voltage for two adjacent coarse tuning values giving the desired

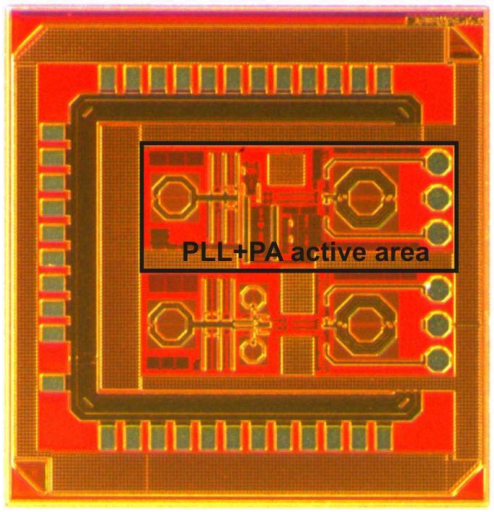

Fig. 4. Die microphotography with a PLL+PA active area of 0.7 mm^2.

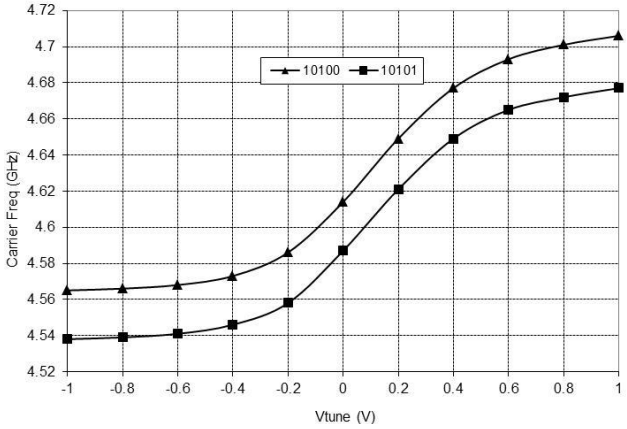

Fig. 5. Tuning curves for two adjacent coarse tuning codes.

4.6-GHz frequency. For the maximal tuning code, the VCO frequency, KVCO gain, and tuning step are 4.3 GHz, 70 MHz/V, and 23 MHz, respectively. For the minimal tuning

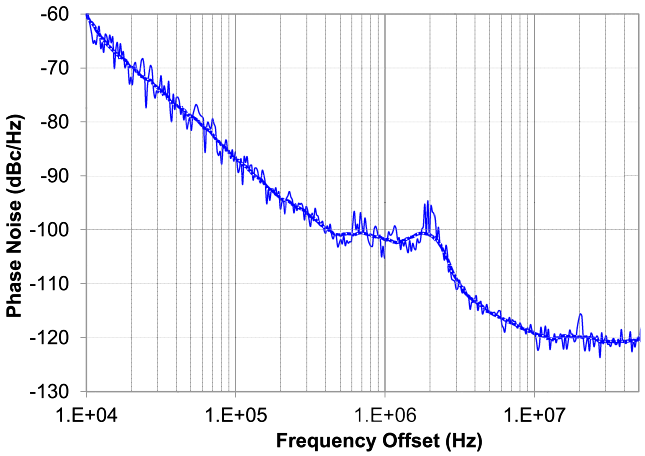

Fig. 6. Measured phase noise of the 4.6-GHz VCO alone, while all other blocks are running.

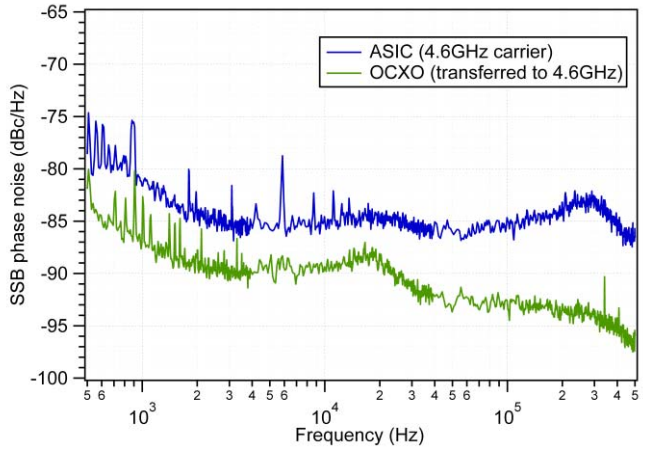

Fig. 7. Phase noise of ASIC output (upper trace) and phase noise of 20-MHz OCXO transferred to 4.6 GHz (lower trace).

code, they are 5.4 GHz, 130 MHz/V, and 40 MHz, respectively. The frequency overlap of neighboring curves is guaranteed with an overlap factor of at least 3.

The measured VCO phase noise is shown in Fig. 6. A level of −91.5 dBc/Hz is obtained at the desired PLL bandwidth of 200 kHz. This result was obtained with all other blocks running (PA, dividers, SDM, PFD, and CP), the only difference being that the PLL filter output differential voltage, normally applied to the VCO, was replaced by the external test voltage. This phase noise measurement takes therefore into account the influence of on-chip noise on the VCO performance. The spurs around 2 MHz are due to on-chip digital noise coupling.

B. Complete PLL Test

The phase noise of the ASIC synthesizer was measured using a phase noise measurement system (model NMS by Spectradynamics inc., [15]). Fig. 7 reports the measured single sideband phase noise at the 4.6-GHz output, reaching −85 dBc/Hz in the band of interest from 2- to 200-kHz offset from carrier (upper trace). This phase-noise level is only slightly higher (4- to max 10-dB higher) than the phase noise of the 20-MHz thermally compensated quartz oscillator (OCXO) transferred to 4.6-GHz carrier (lower trace).

TABLE I
ASIC PERFORMANCE SUMMARY

Parameter	Value	Units
Supply voltage	1.2	Volt
Output frequency	4.6	GHz
Power consumption, Pout = 0 dBm	15	mW
RF output power (single-ended)	-4	dBm
Phase noise, 2-200 kHz from carrier	< -85	dBc/Hz
Phase noise, 1 kHz from carrier	-83	dBc/Hz
Frequency tuning step	0.5	mHz
Frequency tuning resolution	1×10^{-13}	

The RF power was measured at the output using 50-Ω loads to ground on both RF output pads. A maximal single-ended RF power of −4 dBm was measured when the PA was supplied at the maximal LDO voltage of 1.2 V. This corresponds to a differential RF power of 1 dBm. Compared with the expected value of 0 dBm, the 1-dB loss is attributed to losses in the test PCB.

The current consumption of the complete chip, using nominal settings, maximal PA output power and 50-Ω output impedance, is 12.5 mA. This corresponds to 15 mW of power consumption.

C. Frequency Resolution Tests

The frequency tuning resolution was measured using two ASICs whose RF signals are mixed down together. The beating frequency resulting from a slight difference in programming the SDM fractional value can be monitored easily. By programming a frequency difference of 0.5 mHz, a beating at the output with a period of 33 min could be measured, corresponding to a tuning resolution of 1×10^{-13}.

D. Test Summary

The measured performances of the ASIC are summarized in Table I.

V. DESIGN AND TEST OF A COUPLING NETWORK FOR LOW-POWER VCSEL RF CURRENT MODULATION

The low-power operation of a miniature atomic clock mainly depends on an efficient thermal isolation to allow a drastic reduction of the heating energy necessary to operate the alkali vapor cell and the VCSEL at the operating temperature in the range 70 °C–90 °C. This is achieved by using low thermally conductive materials and thin support geometries to connect the heated elements to the clock structure. We present here the design and characterization results of a differential impedance matching network with optimal RF coupling from ASIC to VCSEL and low thermal conductivity, fabricated on a low temperature cofired ceramic (LTCC) substrate. This substrate holds the ASIC (wire-bonded) and the VCSEL, this latter being placed on an island with narrow connecting arms for optimal thermal isolation with the rest of the package.

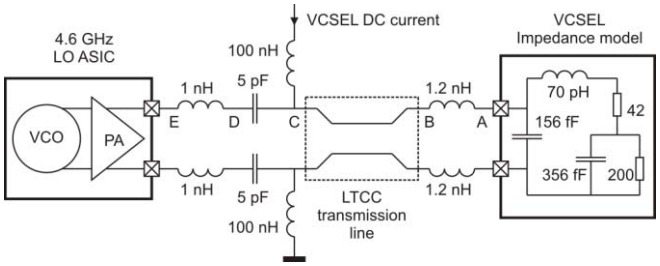

Fig. 8. Schematic diagram of the coupling network from ASIC to VCSEL.

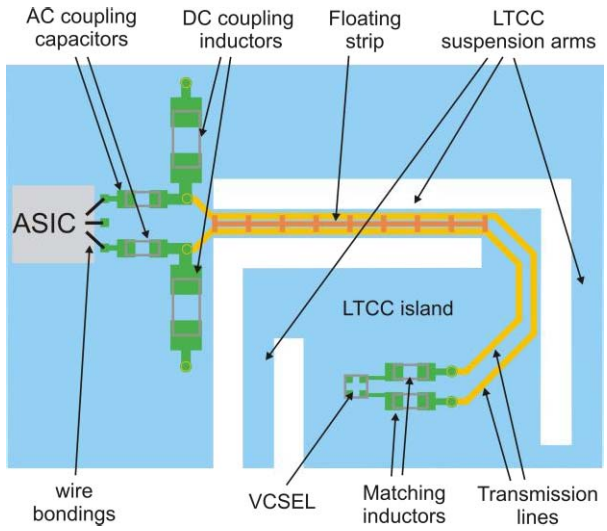

Fig. 9. Layout of the transmission line with passive components.

A. Design

The schematic diagram of the coupling network is shown in Fig. 8. A differential structure is chosen so as to fully use the ASIC differential output power. The network fulfills three different usages: 1) impedance matching between 50-Ω ASIC output and VCSEL input; 2) ac coupling for the ASIC RF signal through a 5-pF capacitor and dc coupling for the VCSEL dc current through a 100-nH inductor; and 3) electrical connection to the VCSEL with low thermal conductivity thanks to a special transmission line. The ASIC bonding wire parasitic inductances are about 1 nH.

The differential transmission line is designed on the LTCC substrate and transmits the RF power through one of the four suspension arms used to isolate thermally the VCSEL island. This is realized using two gold microstrips buried in the LTCC substrate. Their small thickness and width result in very low thermal conduction. The design of the transmission line is shown in Fig. 9, along with the passive components of the network. The ASIC chip is bonded on the left side. Then, the 5-pF ac coupling capacitor and 100-nH inductor are placed next to it (in L-shape). From there are routed the two transmission lines, going through the LTCC suspension arm up to the VCSEL island, connecting to the VCSEL through the 1.2-nH inductors. The length of the transmission line is fixed to 7.8 mm by the geometry of the LTCC substrate. No ground plane is used, resulting in minimal parasitic capacitance. The remaining capacitive behavior of the line is compensated by its U shape, and by adding a floating strip between the

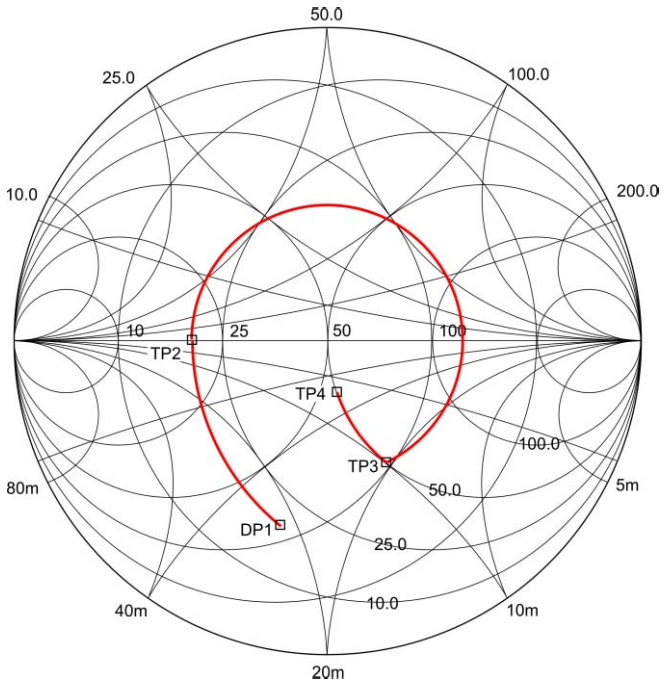

Fig. 10. Smith chart of impedance from VCSEL (DP1) to ASIC (TP4).

transmission lines, at their longest segment, and using another LTCC metal layer. The 45° routing angles are selected for better electromagnetic compatibility. The resulting impedance of the line is 50 Ω.

The impedance matching procedure is done on a single branch of the differential structure. It begins by using the single-ended VCSEL impedance properties [16], and taking half of its differential transform, denoted as point DP1 (impedance of 20-j35 Ω) on the Smith chart of Fig. 10. The capacitive nature of the VCSEL is compensated using a 1.2-nH inductor placed near the VCSEL, resulting in a real impedance of about 20 Ω (point TP2). The transmission line operates an impedance rotation around the 50-Ω point, leading to point TP3 with an impedance of 50-j50 Ω. The ac coupling capacitor and dc coupling inductor values are chosen so as to play negligible role on the impedance at this frequency. The last element is the parasitic inductance of the wire bonding, which reduces the imaginary impedance to about 17 Ω (point TP4). Compared with an ideal impedance of 50 Ω, this results in a transmission loss of about 0.5 dB.

The design is verified using ADS Momentum for the post-layout simulation. After having drawn the transmission line, the S-parameters of the layout as shown in Fig. 9 are extracted, and used in the RF simulation of the complete network with all passive components. At 4.6 GHz, the postlayout simulation performs an insertion loss of 0.88 dB, which is slightly higher than the result from the Smith chart. The fabricated substrate is shown in Fig. 11.

B. Tests With VCSEL

Since it is difficult to characterize the power efficiency of the realized system by direct measurement of the RF power at the VCSEL terminals, the efficiency was characterized by measuring the sideband amplitudes obtained when the

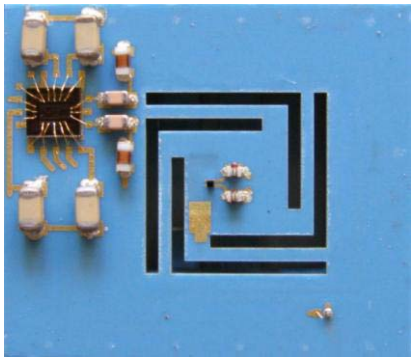

Fig. 11. LTCC substrate with VCSEL island, bonded ASIC, impedance matching network, and transmission line through suspension arm. Overall LTCC substrate size is 14 mm × 16 mm.

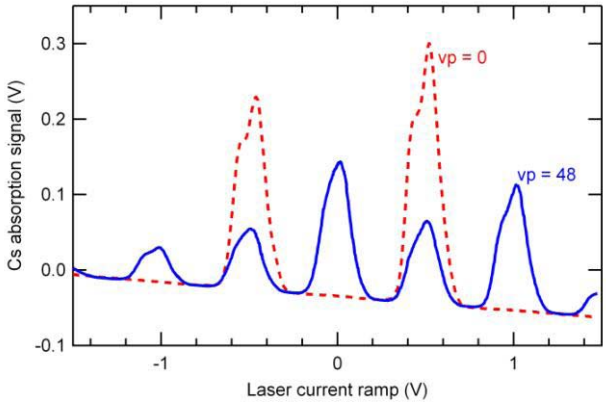

Fig. 12. Cesium cell spectroscopy with two different PA output power settings: vp = 0 corresponds to $-\infty$ dBm, vp = 48 corresponds to -6 dBm.

light from the frequency modulated VCSEL optical signal is absorbed by cesium vapor. For this, an 894.6-nm VCSEL was operated in a setup with a cesium vapor cell heated at its operating temperature. The VCSEL laser beam was collimated and passed through the cell, and the output intensity was measured with a photodetector circuitry. Fig. 12 shows the detector output voltage in function of a ramp voltage applied to the VCSEL current driver to span over the absorption frequencies of cesium. When the ASIC is programmed with minimal RF output power, corresponding to code vp = 0 of the LDO, the two absorption cesium peaks separated by the hyperfine splitting of 9.2 GHz are visible. The irregular peak shape is due to the cesium atomic level structure and the broadening effect of the buffer gas inside the vapor cell. When a differential RF power of about -6 dBm is applied, obtained with code vp = 48 of the LDO, a PA current of 3.2 mA and a reduced VCO current of 1 mA, the effect of the 4.6-GHz modulation is visible. Sideband signals are generated. The first sidebands of the two absorption peaks combine into a central peak with amplitude roughly twice the amplitude of the carrier, denoting good conditions for obtaining a maximal CPT signal. The complete ASIC power consumption in this configuration is 12 mW.

VI. Stability Tests in an Atomic Clock Setup

In order to evaluate the performance of the ASIC in a real application, it was used as RF frequency synthesizer on

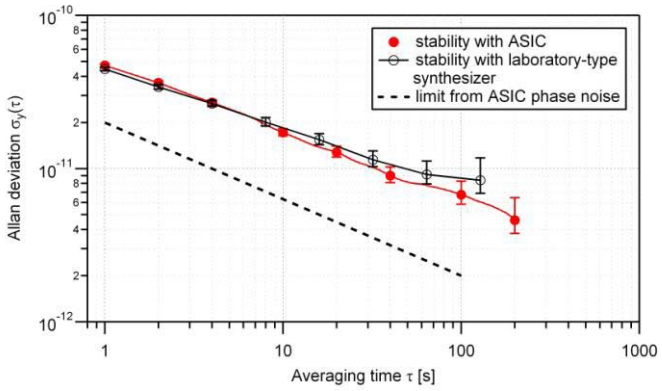

Fig. 13. Clock stabilities recorded with the experimental clock setup, using the reference synthesizer (open symbols) and the ASIC synthesizer (filled symbols). The dashed line is the theoretical limit from ASIC phase noise.

an experimental CPT atomic clock setup described in [17]. In this setup, a distributed feedback laser diode was used instead of a VCSEL, emitting laser radiation at 894.6 nm, in resonance with the Cs D1 optical transition. The modulation sidebands to induce the CPT effect were obtained by modulating the laser beam with a fiber-coupled electro-optical modulator (EOM) driven at 4.6 GHz. The thermal Cs vapor was contained in a microfabricated cell described in [18], confined into a package providing stable temperature and magnetic field conditions. The signal from a photodetector placed behind the physics package was demodulated at $f_m \approx 1$ kHz using a lock-in amplifier (Stanford Research Systems inc., model SR830) and subsequently used to steer the frequency of a 20-MHz OCXO serving as frequency reference for the RF frequency synthesizer.

In order to compare the ASIC performance with a reference RF source, two configurations of quartz oscillator and microwave synthesizer were used. The reference configuration consists of a laboratory-type low-noise frequency synthesizer (spectradynamics inc., model CS-1) including both a 5-MHz quartz oscillator and the 4.6-GHz synthesizer itself, featuring a phase noise at 4.6-GHz carrier of -113 dBc/Hz at 1-kHz offset from carrier, and -126 dBc/Hz at 10–100-kHz offset, which is well below the phase-noise performance of the ASIC synthesizer. The ASIC test configuration consists of a 20-MHz quartz OCXO (Micro Crystal Switzerland, OCXOVT series) and the ASIC synthesizer chip. An additional RF amplifier was connected to amplify the output power of the ASIC to the +3-dBm power level required to drive the EOM. In both configurations, an external frequency generator was used to produce the $f_m \approx$ 1-kHz modulation frequency for the microwave signal, while the modulation depth was set in the respective microwave synthesizer used.

Fig. 13 shows the clock stabilities recorded with the two synthesizer configurations. Both the clock stability obtained with the reference synthesizer (open symbols) and the clock stability obtained with the ASIC synthesizer chip (filled symbols) show a stability of 5×10^{-11} at $\tau = 1$ s and down to $\approx 8 \times 10^{-12}$ at $\tau = 100$ s in good agreement with the theoretical stability limit of $\approx 7 \times 10^{-11}\ \tau^{1/2}$ calculated from the signal-to-noise ratio of the CPT signal over the photodetector

TABLE II
COMPARISON WITH OTHER REALIZATIONS

Parameter	[7]	[8]	[9]	This work	Units
Supply voltage	2.8	1.5	nd	1.2	Volt
Fully-integrated	No	Yes	No	Yes	-
10/20 MHz output	Yes	Yes	No	Yes	-
Output frequency	4.6	3.4	3.4	4.6	GHz
DC Power consumption	40	25	6	12	mW
RF output power	nd	0	nd	-4	dBm
Phase noise, 1kHz offset from carrier	nd	-85	-92	-83	dBc/Hz
Freq. tuning resol.	2	1	nd	0.1	$\times 10^{-12}$
Allan dev, τ=1s	5	40	10	5	$\times 10^{-11}$
Allan dev, τ=100s	1	10	2	0.8	$\times 10^{-11}$

photon shot noise [19]. The observed differences between the two stability curves (ASIC and laboratory-type synthesizer) are within the measurement errors and can be attributed to different loop settings. These results show that the performance of the ASIC synthesizer chip is well suited for realizing miniature atomic clocks with excellent frequency stabilities.

In order to estimate the stability limit of a clock in which the ASIC phase noise would represent the highest contribution to clock stability limitation through intermodulation effect, the theoretical stability limit was computed using (1), (2) and the measured ASIC phase noise. The corresponding stability curve of $2 \times 10^{-11}\ \tau^{1/2}$ is shown in Fig. 13. This limit is well below the typical short-term stability specification of $6 \times 10^{-10}\ \tau^{-1/2}$ for miniature atomic clocks [2].

The presented synthesizer scheme for CPT interrogation is compared with other realizations in Table II. The improvements in terms of power consumption and clock stability for equivalent functionality in terms of level of integration and availability of 10/20-MHz output frequency with high frequency tuning resolution, are particularly outlined.

VII. CONCLUSION

A 4.6-GHz frequency synthesizer ASIC for cesium miniature atomic clocks implemented in a 130-nm RF CMOS process is presented. It is based on a fractional-N PLL with a third-order, 40-bit SDM to achieve an output frequency resolution of 1×10^{-13}. The power consumption of the circuit is <15 mW and it occupies a chip area of 0.7 mm^2 (2 mm^2 with the pads). The low phase noise of -85 dBc/Hz in the 2–200-kHz frequency offset from carrier allows a theoretical clock stability limit of $2 \times 10^{-11}\ \tau^{-1/2}$. A dedicated impedance matching network with low thermal conductivity transmission line was designed to transmit the ASIC RF power to a thermally isolated VCSEL. The system showed optimal sideband generation with an ASIC power consumption of 12 mW. The ASIC was then used on an experimental cesium CPT atomic clock setup, and a short term stability of 5×10^{-11} at $\tau = 1$ s was obtained, comparable with the stability obtained on the same setup with a laboratory frequency synthesizer. The circuit shows ideal performance for low-power, mass-production atomic clock systems.

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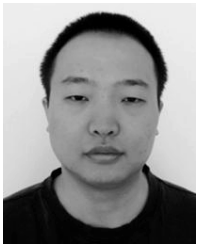

Yazhou Zhao was born in Tianjin, China, in 1984. He received the B.S. degree in microelectronics from Nankai University, Tianjin, in 2006, the M.S. degree in microtechnology from the University of Neuchâtel, Neuchâtel, Switzerland, in 2008, and the Ph.D. degree in low-phase-noise CMOS frequency synthesizers for miniature atomic clocks from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 2013.

His current research interests include low-phase noise, low-power PLL, and VCO design.

Dr. Zhao was the best student paper competition finalist at the IEEE IFCS-EFTF Joint Conference in 2011.

Steve Tanner was born in Orbe, Switzerland, in 1972. He received the M.S. degree in microtechnology from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 1996, and the Ph.D. degree in low-power CMOS image sensors from the University of Neuchâtel, Neuchâtel, Switzerland, in 2000.

He has been with the Electronic and Signal Processing Laboratory, University of Neuchâtel, then with Ecole Polytechnique Fédérale de Lausanne, Lausanne, since 2009, where he was active in analog and digital CMOS IC design, and was a Teacher in Analog and Mixed-Signal IC Design for master's degree students. Since 2005, he has been responsible for the microelectronics group. His current research interests include low-power ADC and DAC design, RF circuits, sensor front ends, and electronics for miniature atomic clocks.

Arnaud Casagrande was born in Bienne, Switzerland, in 1970. He received the M.S. degree in electricity from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 1996.

He has been with the Department of Communication, Asulab, Neuchâtel, Switzerland, a society of the Swatch Group Research and Development, since 1996, where he has been involved in chip and system design. He has authored and co-authored more than 30 patents. His current research interests include low-power RF transceivers and DSPs.

Christoph Affolderbach (M'13) received the Diploma and Ph.D. degrees in physics from the University of Bonn, Bonn, Germany, in 1999 and 2002, respectively.

He has been a Research Scientist with Observatoire Cantonal de Neuchâtel, Neuchâtel, Switzerland, from 2001 to 2006. In 2007, he joined the Laboratoire Temps-Fréquence with the University of Neuchâtel, Neuchâtel, as a Scientific Collaborator. His current research interests include the development of stabilized diode laser systems, atomic spectroscopy, and vapor-cell atomic frequency standards, in particular, laser-pumped high-performance atomic clocks and miniaturized frequency standards.

Dr. Affolderbach is a member of the German Physical Society and the Swiss Physical Society.

Luc Schneller was born in Héricourt, France, in 1983. He received the M.S. degree in microtechnology from Ecole Nationale Supérieure de Mécanique et des Microtechniques, Besançon, France, in 2006, and the Ph.D. degree in space ultrastable quartz oscillator from the University of Franche-Comté, Besançon, in 2009.

He was a Quartz Engineer with Rakon, Paris, France, in 2010. In 2011, he joined the Laboratoire Temps-Fréquence at the University of Neuchâtel, Neuchâtel, Switzerland, where he is involved in miniature atomic clocks.

Gaetano Mileti was born in Saint-Aubin, Switzerland, in 1968. He received the Engineering and Ph.D. degrees in physics from the Swiss Federal Institute of Technology, Lausanne, Switzerland, and the University of Neuchâtel, Neuchâtel, Switzerland, in 1990 and 1995, respectively.

He was a Research Scientist with Observatoire Cantonal de Neuchâtel, Neuchâtel, from 1991 to 1995 and from 1997 to 2006, respectively. From 1995 to 1997, he was with the National Institute of Standards and Technology, Boulder, CO, USA. In 2007, he co-founded the Laboratoire Temps-Fréquence at the University of Neuchâtel, where he is the Deputy Director and an Associate Professor. His current research interests include atomic spectroscopy, stabilized lasers, and frequency standards.

Pierre-André Farine was born in La Chaux-de-Fonds, Switzerland, in 1953. He received the B.Sc. degree in microtechnology from Ecole Technique Supérieur, Neuchâtel, Switzerland, in 1974, and the M.Sc. and Ph.D. degrees in microtechnology from the University of Neuchâtel, Neuchâtel, in 1978 and 1984, respectively.

He was with the Swiss Watch Industries (Swatch Group), Bienne, Switzerland, for 17 years, where he was involved in the development of high-tech products, like pager watches and watches with integrated sensors, such as pressure, compass, altimeter, and temperature. He was also involved in prototype developments for watches with GPSs and cellular phones. Since 2002, he has been a Professor with the Institute of Microtechnology, University of Neuchâtel, then with Ecole Polytechnique Férédale de Lausanne, Lausanne, Switzerland, since 2009, where he leads the Electronic and Signal Processing Laboratory, involved in the study and implementation of low-power solutions for applications covering wireless telecommunications, ultrawideband, global navigation satellite systems, and video and audio processing. He has authored and co-authored more than 40 publications in conferences and technical journals, and holds 45 patent families (more than 240 patents).

Dr. Farine has served as a Program Committee Member and the Program Chair for international conferences.